CLAIMS

1. An interconnect substrate wherein:

a first substrate on which a first interconnect pattern is formed and a second substrate on which a second interconnect pattern is formed are disposed in superimposition;

at least one of the first interconnect pattern and the second interconnect pattern has a mounting region for an electronic chip; and

the first interconnect pattern and the second interconnect pattern are electrically connected.

2. The interconnect substrate as defined in claim 1,

wherein the second substrate is larger than the first substrate, and the whole of the first substrate is adhered to the second substrate.

3. The interconnect substrate as defined in claim 1, wherein:

the first interconnect pattern is formed on one surface of the first substrate;

the second interconnect pattern is formed on one surface of the second substrate; and

a surface of the first substrate opposite to the surface on which the first interconnect pattern is formed and the surface of the second substrate on which the second

interconnect pattern is formed are disposed to oppose each other.

4. The interconnect substrate as defined in claim 3, wherein a plurality of through-holes are formed in the first substrate, and the first interconnect pattern and the second interconnect pattern are electrically connected via the through-holes.

5. The interconnect substrate as defined in claim 4, wherein:

the first interconnect pattern passes over the through-holes;

the through-holes are positioned over the second interconnect pattern; and

a conductive material contacting the first and second interconnect pattern is provided within the through-holes.

6. The interconnect substrate as defined in claim 4, wherein:

the through-holes are positioned over the second interconnect pattern; and

a part of the first interconnect pattern enters the through-holes, and is connected to the second interconnect pattern.

7. The interconnect substrate as defined in claim 4,

wherein a plurality of through-holes are formed in the second substrate, for the formation of a plurality of external terminals electrically connected to the second interconnect pattern and projecting from a surface of the second substrate opposite to the surface on which the second interconnect pattern is formed.

8. The interconnect substrate as defined in claim 7, wherein the through-holes formed in the first substrate and the through-holes formed in the second substrate are formed in communicating positions.

9. The interconnect substrate as defined in claim 8, wherein a part of the second interconnect pattern enters the through-holes formed in the first substrate, and is connected to the first interconnect pattern.

10. The interconnect substrate as defined in claim 8, wherein a part of the first interconnect pattern and a part of the second interconnect pattern project from a surface of the second substrate via the through-holes formed in the second substrate and form external terminals.

11. The interconnect substrate as defined in claim 8, wherein a part of the second interconnect pattern projects into the through-holes formed in the second substrate, avoiding contact with the first interconnect

pattern.

12. The interconnect substrate as defined in any of claims 1 to 11,

wherein the first and second substrates are adhered by an anisotropic conductive film including conductive particles.

13. The interconnect substrate as defined in claim 12,

wherein the first and second interconnect patterns are electrically connected by the conductive particles.

14. An electronic component comprising:

a first substrate on which a first interconnect pattern is formed;

a second substrate having a region which at least a part of the first substrate is disposed opposing, on which a second interconnect pattern is formed electrically connected to the first interconnect pattern; and

at least one electronic chip electrically connected to at least one of the first interconnect pattern and the second interconnect pattern.

15. The electronic component as defined in claim 14,

wherein a surface of the first substrate opposite to a surface on which the first interconnect pattern is formed, and a surface of the second substrate on which the

second interconnect pattern is formed are adhered together.

16. The electronic component as defined in claim 15, wherein a plurality of through-holes are formed in the first substrate, and the first interconnect pattern and the second interconnect pattern are electrically connected via the through-holes.

17. The electronic component as defined in claim 16, wherein:

a plurality of through-holes are formed in the second substrate; and

external terminals electrically connected to the second interconnect pattern via the through-holes formed in the second substrate are provided.

18. The electronic component as defined in claim 17, wherein:

the through-holes formed in the first substrate and the through-holes formed in the second substrate are formed in communicating positions; and

the external terminals contact the second interconnect pattern via the through-holes formed in the second substrate, and are provided on the first interconnect pattern via the through-holes formed in the first substrate.

A2> 19. The electronic component as defined in any of claims 15 to 18, wherein:

an anisotropic conductive film including conductive particles is provided on the surface of the second substrate on which the second interconnect pattern is formed; and

the anisotropic conductive film adheres the first substrate to the second substrate, while also electrically connecting the second interconnect pattern to the electronic chip.

20. The electronic component as defined in claim 19 which comprises first and second electronic chips,

wherein the second substrate is bent to adhere the first electronic chip mounted on the first substrate to the second electronic chip mounted on the second substrate.

A3> 21. A circuit board on which is mounted the electronic component as defined in any of claims 14 to 18.

22. An electronic instrument equipped with the electronic component as defined in any of claims 14 to 18.

23. A method of manufacture of an interconnect substrate comprising:

a disposition step of disposing at least a part of a first substrate on which a first interconnect pattern is

formed to oppose a region of a second substrate on which a second interconnect pattern is formed excluding a mounting region of an electronic chip; and

a connection step of electrically connecting the first and second interconnect patterns.

24. The method of manufacture of an interconnect substrate as defined in claim 23, wherein:

in the disposition step, a surface of the first substrate opposite to a surface on which the first interconnect pattern is formed is adhered to a surface of the second substrate on which the second interconnect pattern is formed; and

a plurality of through-holes are formed in the first substrate, and the first interconnect pattern is formed to pass over the through-holes.

25. The method of manufacture of an interconnect substrate as defined in claim 24, wherein:

before the disposition step, a conductive material is provided on the first interconnect pattern via the through-holes formed in the first substrate; and

when adhering the first substrate to the second substrate in the disposition step, the conductive material is contacted with the second interconnect pattern, whereby the connection step is carried out.

26. The method of manufacture of an interconnect substrate as defined in claim 24,

wherein in the connection step, a part of the first interconnect pattern is bent into the through-holes formed in the first substrate, and connected to the second interconnect pattern.

27. The method of manufacture of an interconnect substrate as defined in claim 24, wherein:

a plurality of through-holes are formed in the second substrate; and

the through-holes formed in the first and second substrates are formed in communicating positions.

28. The method of manufacture of an interconnect substrate as defined in claim 27,

wherein in the connection step, a part of the second interconnect pattern is bent into the through-holes formed in the first substrate, and connected to the first interconnect pattern.

29. The method of manufacture of an interconnect substrate as defined in claim 27,

wherein in the connection step, a part of the first interconnect pattern and a part of the second interconnect pattern are integrally caused to project from a surface of the second substrate via the through-holes formed in the

second substrate, to form external terminals.

30. The method of manufacture of an interconnect substrate as defined in claim 27,

wherein in the connection step, a material for external terminals is contacted with the second interconnect pattern, and provided on the first interconnect pattern via the through-holes formed in the first and second substrates.

A4 31. The method of manufacture of an interconnect substrate as defined in any of claims 23 to 30, wherein:

positioning holes are formed in the first and second substrates; and

before the disposition step, a step is included in which a jig is put into the positioning holes and the first and second substrates are positioned.

32. A method of manufacture of an electronic component comprising:

a disposition step of adhering at least a part of a first substrate on which a first interconnect pattern is formed, having a mounting region for an electronic chip, to a region of a second substrate on which a second interconnect pattern is formed excluding a mounting region for an electronic chip;

a connection step of electrically connecting the

first and second interconnect patterns;

a first mounting step of mounting a first electronic chip to be electrically connected to the first interconnect pattern on the first substrate; and

a second mounting step of mounting a second electronic chip to be electrically connected to the second interconnect pattern on the mounting region of an electronic chip of the second substrate.

33. The method of manufacture of an electronic component as defined in claim 32, wherein:

in the disposition step, a surface of the first substrate opposite to a surface on which the first interconnect pattern is formed is adhered to a surface of the second substrate on which the second interconnect pattern is formed; and

a plurality of through-holes are formed in the first substrate, and the first interconnect pattern is formed to pass over the through-holes.

34. The method of manufacture of an electronic component as defined in claim 33, wherein:

a plurality of through-holes are formed in the second substrate; and

the through-holes formed in the first and second substrates are formed in communicating positions.

35. The method of manufacture of an electronic component as defined in claim 34,

wherein in the connection step, a material for external terminals is contacted with the second interconnect pattern, and provided on the first interconnect pattern via the through-holes formed in the first and second substrates.

36. The method of manufacture of an electronic component as defined in claim 32,

wherein in the disposition step and the second mounting step, an anisotropic conductive film including conductive particles is provided on a surface of the second substrate on which the second interconnect pattern is formed, and the first substrate is adhered to the second substrate by means of the anisotropic conductive film, while electrically connecting the second interconnect pattern to the second electronic chip.

37. The method of manufacture of an electronic component as defined in claim 32, further comprising:

a step in which the second substrate is bent to adhere the first electronic chip mounted on the first substrate to the second electronic chip mounted on the second substrate.

A5> 38. The method of manufacture of an electronic component

Cont A5 as defined in any of claims 32 to 37,

wherein the disposition step is carried out after the first mounting step.

39. The method of manufacture of an electronic component as defined in claim 38, wherein:

the second substrate is a part of a flexible substrate; and

the second substrate is formed by stamping out the flexible substrate after the disposition step.